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EXAMINER	
MATTHEW, AARON D	

ART UNIT	PAPER NUMBER
2114	

DATE MAILED: 03/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/056,393	VENKATRAMAN ET AL.	
	Examiner	Art Unit	
	Aaron D Matthew	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 January 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11,13-18 and 23-30* is/are pending in the application.

4a) Of the above claim(s) *29 and 30* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11,13-18 and 23-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 12 and 19-22 have been cancelled.

2. Claims 29 and 30 have been withdrawn from consideration.

3. Claims 1-11, 13-18, and 23-28 have been examined and are discussed below.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 3-5, and 9-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hoskins, (US 2001/0042223), and further in view of Crouch et al, (US 5,995,731).

Regarding claim 1, Hoskins teaches a method comprising:

- Testing a memory to determine a location of a bad memory cell, (see par. 0015, lines 4-7: discovering a defective memory cell inherently requires some means of testing said cell), wherein the memory is organized into one or more

clusters, each of the one of more clusters having one or more memory blocks, (see par. 0042, lines 1-6, wherein the memory is divided into a set of tracks {clusters} each comprising a number of sectors, and note par. 0003 wherein a sector is a memory block comprising memory cells);

- Mapping out an address location associated with the bad memory cell, (note par. 0009, lines 1-4; wherein mapping defective sectors to a good sector is considered synonymous with mapping out the defective sector); and
- Offsetting one or more physical address locations associated with one or more good memory cells so that logical addressing is linear and the memory appears contiguous, (see par. 0058, lines 5-9, and note Fig. 8).

Hoskins fails to teach that the step of testing the memory includes one or more controllers operating in parallel to test at least some of the one or more memory blocks at the same time.

Crouch teaches a method of testing a memory wherein one or more controllers operate in parallel to test at least some of the one or more memory blocks at the same time, (see col. 3, lines 40-51).

Crouch and Hoskins are analogous art because they are from the same field of endeavor, viz., memory test systems.

At the time of applicant's invention, one of ordinary skill in the art would have considered it obvious to combine the one or more controllers operating in parallel to test at least some of the one or more memory blocks at the same time, as taught in Crouch, with the memory testing method disclosed in Hoskins.

One of ordinary skill in the art would have been motivated to combine the teachings because there is a well recognized need in the art to improve existing methods by reducing the time it takes to achieve similar results. Crouch shows that testing a memory in parallel, rather than solely sequentially, saves the overall amount of time required for testing, (see col. 3, lines 1-6). One of ordinary skill in the art, in view of Crouch, would have been properly motivated to use one or more controllers to test at least some of the one or more memory blocks in parallel, in Hoskins, in order to reduce the amount of time required to complete the testing.

Regarding claims 3 and 9, Hoskins teaches a method, as disclosed in reference to claim 1, wherein:

- One or more bad memory cells are located within one or more respective memory blocks, (it is inherent, in determining that one or more memory blocks are defective, note par. 0015, that said memory blocks contain one or more bad memory cells); and

- Mapping out of the address location associated with the bad memory cell includes mapping out one or more respective memory blocks, (sectors), having the one or more bad memory cells, (note, again, par. 0058, lines 5-9, and note Fig. 8, wherein a sector having a bad memory cell is mapped out).

Regarding claims 4 and 5, again note Fig. 8, wherein offsetting one or more physical address locations associated with the one or more good memory cells is by one memory block, (sector), and thus, the corresponding size of addressable space of said memory block having the bad memory cell. Note also that each of the one or more good memory cells, shown addressable in ascending order after the memory block having the bad memory cell, has its one or more physical address locations offset, (signified by the corresponding logical address); by the size of addressable space in a memory block to linearize the logical addressing.

Regarding claim 10, note, again, Fig. 8, wherein offsetting the one or more physical address locations, (i.e. the slipping of the LBA, see par. 0058), associated with the one or more good memory cells is by one or more memory blocks, (sectors), associated with the number of one or more respective memory blocks having the one or more bad memory cells and the corresponding size of addressable space of the one or more memory blocks, (the size of addressable space of a sector disclosed as 512 bytes, see par. 0003, the sector itself being addressable).

5. Claims 11, and 13-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hoskins, and further in view of Sugibayashi, (US 5,848,021), and Crouch.

Regarding claim 11, Hoskins teaches a reconfigurable memory comprising:

- An array of data sectors, each comprising an array of memory cells, (see par. 0003), wherein the array of memory cells is organized into one or more clusters, each of the one or more clusters having one or more memory blocks, (see par. 0042, lines 1-6, wherein the memory is divided into one or more tracks, (clusters), each comprising one or more sectors, and note par. 0003 wherein a sector is a memory block comprising an array of memory cells).
- A reconfigurable memory controller, (see par. 0048), to receive a logical address and generate a physical address to address the array of memory cells, the reconfigurable memory controller to map out one or more physical addresses of words, (sectors), having one or more bad memory cells, (a defective sector, comprising an array of memory cells, inherently comprises one or more defective memory cells), to form a linear logical address space without addresses to words of the one or more bad memory cells, (see par. 0058 and Fig. 8).

Hoskins teaches a disc drive comprising said reconfigurable memory, but fails to teach an integrated circuit comprising said reconfigurable memory.

Sugibayashi teaches an integrated circuit comprising a reconfigurable memory for mapping out defective memory cells.

At the time of applicant's invention, one of ordinary skill in the art would have considered it obvious to combine the memory reconfiguration technique of Hoskins with the integrated circuit memory device of Sugibayashi in order to achieve an integrated circuit comprising a reconfigurable semiconductor memory utilizing the memory reconfiguration techniques of Hoskins.

One of ordinary skill in the art would have been motivated to combine the teachings because the integrated circuit of Sugibayashi meets an implicit need in the art of memory devices, by improving memory access speeds. One of ordinary skill in the art would have clearly recognized that the use of magnetic disk drives and semiconductor memory devices is prevalent in the art, and that both devices are direct substitutes in most applications, (note Sugibayashi, col. 1, lines 16-20). Moreover, Hoskins and Sugibayashi both disclose a need for techniques to reconfigure partially defective memory, and one of ordinary skill in the art would have clearly recognized that techniques for remapping defective memory blocks, as disclosed in Hoskins, are directly applicable to the partially defective semiconductor

memory of Sugibayashi. Therefore, one of ordinary skill in the art would have clearly recognized the substitutability of a semiconductor memory device for the disk drive of Hoskins, and would have been motivated to utilize the integrated circuit comprising said reconfigurable semiconductor memory device to improve memory access speeds.

Hoskins, in view of Sugibayashi, fails to teach that the integrated circuit further comprises a built in self tester including one or more controllers that operate in parallel to test at least some of the one or more memory blocks at the same time. However, Sugibayashi does teach a built in self tester, (see col. 10, lines 19-28, and Fig. 5, element 23d).

Crouch teaches an integrated circuit comprising a built in self tester, which includes one or more controllers that operate in parallel to test at least some of the one or more memory blocks at the same time, (see col. 3, lines 40-51).

Crouch, Hoskins, and Sugibayashi are analogous art because they are from the same field of endeavor, viz., memory test systems.

At the time of applicant's invention, one of ordinary skill in the art would have considered it obvious to combine the one or more controllers operating in parallel to

test at least some of the one or more memory blocks at the same time, as taught in Crouch, with the memory testing method disclosed in Hoskins.

One of ordinary skill in the art would have been motivated to combine the teachings because there is a well recognized need in the art to improve existing methods by reducing the time it takes to achieve similar results. Crouch shows that testing a memory in parallel, rather than solely sequentially, saves the overall amount of time required for testing, (see col. 3, lines 1-6). One of ordinary skill in the art, in view of Crouch, would have been properly motivated to use one or more controllers to test at least some of the one or more memory blocks in parallel, in Hoskins, in order to reduce the amount of time required to complete the testing.

Regarding claim 13, see Hoskins, Fig. 8, and note that the sectors, as described in Hoskins, can be interpreted both as words and as memory blocks each comprising an array of memory cells.

Regarding claim 14, Hoskins-Crouch fails to teach that the reconfigurable memory controller includes a configuration register associated with each memory block, each configuration register including a memory block enable bit, the memory block enable bit to map out the respective memory blocks having the bad memory cells.

However, Hoskins-Crouch does teach maintaining a reserve sector on the disk drive, associated with each memory block, used to store and retrieve information required for the disc drive controller to manage and control the storage and retrieval of information in the disc drive, (see Hoskins, par. 0050).

Sugibayashi teaches a semiconductor memory device used to map out defective memory blocks, wherein a reconfigurable memory controller, (see Fig. 3, 7d), includes a configuration register including a memory block enable bit, the memory block enable bit to map out the respective memory blocks having the bad memory cells, (see col. 4, lines 17-30; the plurality of memory units and memory cell groups corresponding to configuration registers and memory blocks respectively; also note col. 7, lines 34-51 wherein the control data information is a memory block enable bit).

At the time of applicant's invention, one of ordinary skill in the art would have considered it obvious to combine the teachings in order to achieve a reconfigurable memory controller in a semiconductor memory device, as disclosed in Sugibayashi, that utilizes the advantages taught in Hoskins-Crouch in creating a linear logical address space in a partially defective memory device.

One of ordinary skill in the art would have been motivated to combine the teachings because the configuration registers, taught in Sugibayashi, meet a need in common

with the reserve sectors of Hoskins, in providing the memory controller with reconfiguration information, and offer a further advantage of improving access times for said information, (see Sugibayashi, col. 3, lines 52-58). One of ordinary skill in the art would have also clearly recognized that the use of magnetic disk drives and semiconductor memory devices is prevalent in the art, and that both devices are direct substitutes in most applications, (note Sugibayashi, col. 1, lines 16-20). Moreover, Hoskins-Crouch and Sugibayashi both disclose a need for techniques to reconfigure partially defective memory, and one of ordinary skill in the art would have clearly recognized that techniques for remapping defective memory blocks, as disclosed in Hoskins-Crouch, are directly applicable to the partially defective semiconductor memory of Sugibayashi. Therefore, one of ordinary skill in the art would have clearly recognized the substitutability of a semiconductor memory device for the disk drive of Hoskins-Crouch, and would have been motivated to utilize the configuration registers disclosed in Sugibayashi in place of the reserve sectors of Hoskins to improve access times for the information stored therein.

Regarding claims 15-17, Sugibayashi teaches a reconfigurable memory, as discussed in reference to claim 14, wherein:

- Each configuration register further includes a base address associated with one or more upper address bits of an address to begin the physical addressing of a respective memory block having all good memory cells, (note

col. 4 lines 35-40, wherein physical addressing of non-defective memory blocks is assigned through the configuration registers, and note col. 6, lines 32-55, wherein this physical base address is associated with one or more upper address bits of an address);

- A value of the base address is compared with a value of the one or more upper address bits of the address to determine if each memory block having all good memory cells is selected for access, (note col. 4, lines 35-40, wherein a memory block is selectively enabled upon a successful comparison of the base address and said one or more upper address bits); and
- For a given memory block the comparison between the value of the base address and the value of the one or more upper address bits of the address results in a match and the given memory block is selected for access, (note col. 4, lines 55-58 wherein a logical address selects a given, non-defective memory block for access upon comparison with said base address).

Regarding claim 18, Sugibayashi teaches that each memory block is a self contained memory unit, (see Fig. 5), including an array of memory cells, (see col. 4, lines 17-21), an address decoder, (see Fig. 5, elements 22c and 22d), sense amplifier array, (see Fig. 5, element 21c), and tri-state bus drivers, (see col. 10, lines 45-50).

6. Claims 2, and 23-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hoskins, in view of Crouch et al, (hereinafter referred to as Hoskins-Crouch), as applied to claims 1 and 11 above, and further in view of Sugibayashi, (U.S. 5,848,021).

Regarding claim 2, Hoskins-Crouch teaches that the testing is self-testing performed by a built in self tester, wherein the self tester includes the one or more controllers, (see Crouch, col. 3, lines 1-6 and 40-51).

Hoskins also teaches a disc drive comprising said memory, but fails to teach an integrated circuit comprising said memory, wherein testing is performed on chip.

Sugibayashi teaches a method of reconfiguring a partially defective memory wherein the memory is within an integrated circuit and the testing is self-testing performed on chip by a built in self tester, (see col. 10, lines 19-28, and Fig. 5, element 23d).

At the time of applicant's invention, one of ordinary skill in the art would have considered it obvious to combine the teachings in order to achieve a method of reconfiguring a partially defective memory within the integrated circuit of Sugibayashi, that utilizes the advantages taught in Hoskins in creating a linear logical address space in a partially defective memory and the advantages of

Sugibayashi in using on chip self testing to determine the defective locations in the memory.

One of ordinary skill in the art would have been motivated to combine the teachings because the integrated circuit of Sugibayashi meets an implicit need in the art of memory devices, by improving memory access speeds. One of ordinary skill in the art would have clearly recognized that the use of magnetic disk drives and semiconductor memory devices is prevalent in the art, and that both devices are direct substitutes in most applications, (note Sugibayashi, col. 1, lines 16-20). Moreover, Hoskins and Sugibayashi both disclose a need for techniques to reconfigure partially defective memory, and one of ordinary skill in the art would have clearly recognized that techniques for remapping defective memory cells, as disclosed in Hoskins, are directly applicable to the partially defective semiconductor memory of Sugibayashi. Therefore, one of ordinary skill in the art would have clearly recognized the substitutability of a semiconductor memory device for the disk drive of Hoskins, and would have been motivated to utilize the integrated circuit comprising said reconfigurable semiconductor memory device to improve memory access speeds. The on-chip, self-testing of Sugibayashi offers further motivation to combine the teachings by reducing the time and costs involved in testing semiconductor memory devices during manufacture.

Regarding claim 23, see Hoskins, par. 0048, wherein the reconfigurable memory controller includes a memory block base address, (note lines 5-7).

Regarding claim 24, note that the integrated circuit of Sugibayashi is operable specifically as a reconfigurable semiconductor memory device, (see Abstract), and, as such, is an application specific integrated circuit.

Regarding claims 25-28, Sugibayashi teaches that said integrated circuit further comprises:

- A host port, (see col. 10, lines 19-23 and note col. 9, lines 55-59 wherein the external device is disclosed as a host);
- A memory test register, (col. 12, line 8);
- A test access port, (see col. 10, lines 23-28).

7. Claims 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hoskins, in view of Crouch et al, (hereinafter referred to as Hoskins-Crouch), as applied to claim 1 above, and further in view of Lin et al, (U.S. 6,141,768).

Regarding claim 7, Hoskins-Crouch fails to teach that testing the memory includes:

- Writing one or more test patterns into memory cells in the memory;

- Reading out data from the memory cells; and
- Comparing the read out data with an expected pattern of the one or more test patterns to determine a location of the bad memory cell.

However, Hoskins-Crouch does teach identifying newly-defective sectors during operation of the disc drive, (see Hoskins, par. 0090), which inherently requires testing of the memory, and further discloses that error detection operations comprising writing to the memory cells, reading from the memory cells, and performing appropriate operations upon the retrieved data, (see Hoskins, par. 0041).

Lin teaches a self-corrective memory system which is reconfigurable upon detection of defective memory cells, and performs self testing upon the memory, including:

- Writing a test pattern into the memory cells; and
- Verifying the accuracy of the results, (see col. 1, lines 49-54), which inherently includes:
    - Reading out data from the memory cells; and
    - Comparing the read out data with an expected pattern to determine the location of the bad memory cell.

At the time of applicant's invention, one of ordinary skill in the art would have considered it obvious to combine the memory self-testing method of Lin, with the memory reconfiguration method of Hoskins-Crouch in order to achieve a means of detecting defective memory cells which was not explicitly stated in Hoskins-Crouch.

One of ordinary skill in the art would have been motivated to combine the teachings because Lin teaches a method of self-testing that was not explicitly stated in Hoskins-Crouch, but meets an explicitly stated need in Hoskins of detecting defective memory cell locations. Hoskins-Crouch teaches that error detection operations should be performed to locate defective memory locations, but fails to teach a specific means of performing said error detection. Therefore, one of ordinary skill in the art would have been motivated to use the method of Lin, (see col. 1, lines 49-50, in which Lin discloses said testing procedure as a "known testing procedure"), in order to enable the error detection needed in the memory reconfiguration method of Hoskins-Crouch.

Regarding claim 8, see Hoskins, Fig. 8, wherein the location of a bad memory cell is associated with a "PCHS" address.

8. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hoskins, in view of Crouch, (hereinafter referred to as Hoskins-Crouch), as applied to claims 1 and 3 above, and further in view of Lo et al, (U.S. 4,922,451), and Beausoliel, (U.S. 3,735,368).

Hoskins-Crouch fails to teach that the memory discussed in reference to claims 1 and 3 has four clusters each having four memory blocks and each memory block containing 512 kilobits of memory cells. However, Hoskins-Crouch does teach that each memory device is to have a number of tracks, (clusters), appropriate to constraints of the medium hosting said tracks, (see Fig. 3), and each comprising a plurality of sectors with 512 bytes of memory cells.

Beausoliel teaches a reconfigurable memory device organized into four clusters each having four memory blocks, (see Fig. 1, elements 16 and 18 respectively).

Beausoliel teaches that each memory block contains 256 bits of memory cells, (see col. 4, lines 4-5), but fails to teach that each memory block contains 512 kilobits of memory cells.

Lo teaches a method for remapping partially defective memory wherein a memory comprises a plurality of memory blocks and each memory block contains 512 kilobits, (64 kilobytes), of memory cells, (see col. 4, lines 18-26).

Lo, Beausoliel and Hoskins-Crouch are analogous art because they are from the same field of endeavor, viz., reconfiguring partially defective memory.

At the time of applicant's invention, one of ordinary skill in the art would have considered it obvious to combine the teachings of Beausoliel and Lo with the memory reconfiguration method of Hoskins-Crouch in order to achieve a reconfigurable memory comprised of four clusters each having four memory blocks, (as in Beausoliel), and each memory block containing 512 kilobits of memory cells, (as in Lo).

One of ordinary skill in the art would have been motivated to combine the teachings because Hoskins-Crouch teaches that the number of tracks, (clusters), per memory, and sectors, (memory blocks), per track are often determined by one skilled in the art based on the constraints of the memory device, (note par. 0042). Therefore, in view of Beausoliel and Lo, one of ordinary skill in the art would have considered it obvious to partition a memory into four clusters with four memory blocks each containing 512 kilobits of memory cells, utilizing the methods of Hoskins-Crouch, based upon a preference and the constraints of the memory device being used.

Response to Arguments

9. Claims 12, and 19-22 have been cancelled.

10. Applicant's arguments, see page 11, filed 1/13/2005, with respect to the objections to the specification and the claims have been fully considered and are persuasive. The objection to the specification, and claims 12 and 20, have been withdrawn.

11. Applicant's arguments, see pages 11-12, filed 1/13/2005, with respect to the rejections under 35 U.S.C. 112, second paragraph, have been fully considered and are persuasive. The rejection of claim 10, under 35 U.S.C. 112, second paragraph, has been withdrawn.

12. Applicant's arguments with respect to 35 U.S.C. 102(e) and 103(a) rejections to claims 1-11, 13-18 and 23-28 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aaron D Matthew whose telephone number is (571) 272-3662. The examiner can normally be reached on Mon-Fri, from 8:00 am - 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert W Beausoliel can be reached on (571) 272-3645. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Aaron D Matthew
Examiner
Art Unit 2114

ADM

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